

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for monitoring a tunnel oxide layer, the method comprising:

5 (a) providing a semiconductor substrate, and forming at least one memory cell on a surface of the semiconductor substrate, the memory cell comprising a first gate, a second gate, and the tunnel oxide layer from top to bottom in a stack;

10 (b) electrically connecting the first gate and the second gate;

(c) applying a first gate voltage to the first gate, the first gate voltage being a swing time-dependent DC ramping voltage;

15 (d) measuring a first gate leakage current of the memory cell to calculate a first constant from an equation;

(e) applying a second gate voltage to the first gate, the second gate voltage being a swing time-dependent DC ramping voltage;

20 (f) measuring a second gate leakage current of the memory cell to calculate a second constant from the equation;

(g) calculating a first ratio of the second constant to the first constant; and

25 (h) performing a comparing step to compare the value of the first ratio with a predetermined value.

2. (Currently amended) The method of claim 1 wherein
30 the semiconductor substrate is a silicon substrate of a semiconductor wafer and the memory cell is formed in the testing area of the semiconductor wafer.

3. (Original) The method of claim 1 wherein the memory cell is a flash memory cell, the first gate and the second gate are a controlling gate and a floating gate
5 of the flash memory cell respectively.

4. (Original) The method of claim 1 wherein the memory cell is a non-volatile memory cell, the first gate and the second gate are a controlling gate and a floating
10 gate of the non-volatile memory cell respectively.

5. (Original) The method of claim 1 wherein the quality of the tunnel oxide layer is degenerated to be not acceptable when the value of the first ratio is greater
15 than the predetermined value.

6. (Currently amended) The method of claim 1 wherein the equation is the Fowler-Nordeheim tunneling mechanism equation.
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7. (Original) The method of claim 1 wherein the predetermined value is 10.

8. (Original) The method of claim 1 wherein each
25 constant is a . value corresponding to each gate
voltage respectively.

9. (Currently Amended) The method of claim 8 wherein the first constant is a .1 value corresponding to the
30 first gate voltage, and the .1 value is equal to $\left\{ \Delta \ln \left[\frac{\text{the first gate leakage current}}{\left(\left| \text{the first gate voltage} \right| - \left| \text{a flatband voltage} (V_{fb}) \right| \right)^2} \right] \right\} \div \left\{ \Delta \left[1 \div \left(\left| \text{the} \right. \right. \right. \right.$

first gate voltage $| - |$ the flatband voltage $|) |$ } }]] .

10. (Currently amended) The method of claim 8 wherein the second constant is a .2 value corresponding to the
 5 second gate voltage, and the .2 value is equal to $\left[\left\{ \Delta \ln \left[\left| \frac{\text{the second gate leakage current}}{\left(\left| \text{the second gate voltage} - \left| \text{the flatband voltage} (V_{fb}) \right| \right)^2} \right| \right] \right\} \div \left\{ \Delta \left[1 \div \left(\left| \text{the second gate voltage} - \left| \text{the flatband voltage} \right| \right) \right] \right\} \right] \right\} .$

10 11. (Currently amended) The method of claim 8 further comprises the following steps when the value of the first ratio is not greater than the predetermined value:

15 applying a third gate voltage to the first gate, the third gate voltage is a swing time-dependent DC ramping voltage;

measuring a third gate leakage current of the memory cell to calculate a third constant from the equation;
 calculating a second ratio of the third constant
 20 to the second constant; and

performing the comparing step to compare the value of the second ratio with the predetermined value.

12. (Original) The method of claim 11 wherein the steps
 25 (c) to (h) are repeated when the value of the second ratio is not greater than the predetermined value.

13. (Original) The method of claim 11 wherein the quality of the tunnel oxide layer is degenerated to
 30 be not acceptable when the value of the second ratio is greater than the predetermined value.

14. (Currently amended) The method of claim 11 wherein the third constant is a .3 value corresponding to the third gate voltage, and the .3 value is equal to $\left[\frac{\Delta \ln[| \text{the third gate leakage current} | / (| \text{the third gate voltage} | - | \text{a flatband voltage}(V_{fb}) |)^2]}{\Delta [1 / (| \text{the third gate voltage} | - | \text{the flatband voltage} |)]} \right]$.

15. (Currently amended) The method of claim 14 further comprising a step for plotting a $-V_g$ curve of each . value respectively corresponding to the first gate voltage, the second gate voltage and the third gate voltage versus the first gate voltage, the second gate voltage and the third gate voltage, a reference $-V_g$ curve for the unstress-induced tunnel oxide layer in the memory cell is compared with the $-V_g$ curve to monitor the quality of the tunnel oxide layer.

16. (Original) The method of claim 15 wherein the $-V_g$ curve comprises at least a first region (region I), a second region (region II), and a third region (region III).

17. (Original) The method of claim 16 wherein the . value within the first region is zero to represent each gate leakage current flowing through the first gate and the second gate in the memory cell being less than a predetermined current value, the absolute value of the . value within the second region increases to represent the stress-induced leakage current (SILC) resulting in the increase of each gate leakage current of the memory cell, the . value within the third region crosses the reference $-V_g$ curve to represent a

plurality of carriers being trapped by the tunnel oxide layer.

18.(Original) The method of claim 17 wherein the
5 predetermined current value is $1.0 \times 10^{-11} \text{A}$.

19.(Currently amended) The method of claim 8 further
comprising a step for plotting a $-V_g$ curve of each
. value versus each gate voltage, a reference $-V_g$ curve
10 for the unstress-induced tunnel oxide layer in the
memory cell is compared with the $-V_g$ curve to monitor
the quality of the tunnel oxide layer.

20.(Original) The method of claim 1 wherein the method
15 is applied to a wafer acceptance testing (WAT)
equipment to fast monitor the stress-induced
degradation of the tunnel oxide layer in the memory
cell.

20 21.(Currently amended) A method for fast monitoring
the stress-induced degradation of an oxide layer by
a wafer acceptance testing (WAT) equipment, the method
comprising:

(a) providing a ~~semiconductor~~ substrate, a surface
25 of the ~~semiconductor~~ substrate comprising the oxide
layer and a first gateconductive layer disposed on the
oxide layer;

(b) applying a first ~~gate~~-voltage to the first
gateconductive layer, the first ~~gate~~-voltage being a
30 swing time-dependent DC ramping voltage;

(c) measuring a first ~~gate~~-leakage current flowing
through the first gateconductive layer to calculate

a first proportional value from the first ~~gate-voltage~~, the first ~~gate-leakage~~ current, and an equation, the first proportional value corresponding to the first ~~gate-voltage~~;

5 (d) applying a second ~~gate-voltage~~ to the first gateconductive layer, the second ~~gate-voltage~~ being a swing time-dependent DC ramping voltage;

(e) measuring a second ~~gate-leakage~~ current flowing through the first gateconductive layer to calculate
10 a second proportional value from the second ~~gate-voltage~~, the second ~~gate-leakage~~ current, and the equation, the second proportional value corresponding to the second ~~gate-voltage~~; and

(f) calculating a first ratio of the second
15 proportional value to the first proportional value.

22. (Currently amended) The method of claim 21 wherein the ~~semiconductor~~ substrate is a silicon substrate of a semiconductor wafer and the first gateconductive layer is formed in ~~thea~~ testing area of the
20 semiconductor wafer.

23. (Currently amended) The method of claim 21 wherein a second gateconductive layer is formed between the
25 first gateconductive layer and the oxide layer.

24. (Currently amended) The method of claim 23 further comprises ing an electrically connecting step performed before applying the first ~~gate-voltage~~ to
30 the first gateconductive layer to electrically connect the first gateconductive layer and the second gateconductive layer.

25. (Currently amended) The method of claim 24 wherein
the ~~memory cell is a flash memory cell~~, the first
gateconductive layer and the second gateconductive
5 layer are a controlling gate and a floating gate of
thea flash memory cell respectively, and the oxide
layer is a tunnel oxide layer of the flash memory cell.

26. (Currently amended) The method of claim 24 wherein
10 the first gateconductive layer is a controlling gate
of ~~the flash~~ non-volatile memory cell, the second
gateconductive layer is a floating gate of the flash
non-volatile memory cell, the oxide layer is a tunnel
oxide layer of the flash non-volatile memory cell.

15 27. (Currently amended) The method of claim 21 wherein
the first gateconductive layer is a gate of a
metal-oxide-semiconductor (MOS) transistor, the oxide
layer is a gate oxide layer of the MOS transistor.

20 28. (Currently amended) The method of claim 21 further
comprisesing a comparing step to compare the value of
the first ratio with a predetermined value.

25 29. (Currently amended) The method of claim 28 wherein
the quality of the ~~tunnel~~-oxide layer is degenerated
to be not acceptable when the value of the first ratio
is greater than the predetermined value.

30 30. (Original) The method of claim 28 wherein the
predetermined value is 10.

31. (Currently amended) The method of claim 21 wherein the equation is the Fowler-Nordeheim tunneling mechanism equation.

5 32. (Currently amended) The method of claim 21~~8~~ wherein each proportional value is a . value corresponding to each ~~gate~~-voltage respectively.

33. (Currently amended) The method of claim 32 wherein
10 the first proportional value is a .1 value corresponding to the first ~~gate~~-voltage, and the .1 value is equal to $\left[\frac{\Delta \ln[| \text{the first } \text{gate-leakage current} | / (| \text{the first } \text{gate-voltage} | - | \text{a flat band voltage}(V_{fb}) |)^2]}{\Delta [1 + (| \text{the first } \text{gate voltage} | - | \text{the flatband voltage} |)]} \right]$.
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34. (Currently amended) The method of claim 32 wherein the second proportional value is a .2 value corresponding to the second ~~gate~~-voltage, and the .2
20 value is equal to $\left[\frac{\Delta \ln[| \text{the second } \text{gate-leakage current} | / (| \text{the second } \text{gate-voltage} | - | \text{the flatband voltage}(V_{fb}) |)^2]}{\Delta [1 + (| \text{the second } \text{gate voltage} | - | \text{the flatband voltage} |)]} \right]$.

25 35. (Currently amended) The method of claim 32 further comprises~~ing~~ the following steps when the value of the first ratio is not greater than the predetermined value:

applying a third ~~gate~~-voltage to the first
30 ~~gate~~conductive layer, the third ~~gate~~-voltage is a swing time-dependent DC ramping voltage;

measuring a third ~~gate~~-leakage current flowing through the first ~~gate~~conductive layer;

calculating a third proportional value from the third ~~gate~~-voltage, the third ~~gate~~-leakage current, and the equation, the third proportional value corresponding to the third ~~gate~~-voltage;

calculating a second ratio of the third proportional value to the second proportional value; and

10 performing the comparing step to compare the value of the second ratio with the predetermined value.

36. (Original) The method of claim 35 wherein the steps (b) to (f) are repeated when the value of the second ratio is not greater than the predetermined value.

37. (Original) The method of claim 35 wherein the quality of the oxide layer is degenerated to be not acceptable when the value of the second ratio is greater than the predetermined value.

38. (Currently amended) The method of claim 35 wherein the third proportional value is a .3 value corresponding to the third ~~gate~~-voltage, and the .3 value is equal to $\left[\left\{ \Delta \ln \left[\frac{|\text{the third gate-leakage current}|}{(|\text{the third gate-voltage}| - |\text{a flatband voltage}(V_{fb})|)^2} \right] \right\} \div \left\{ \Delta [1 + (|\text{the third gate voltage}| - |\text{the flatband voltage}|)] \right\} \right]$.

39. (Currently amended) The method of claim 38 further comprising a step for plotting a $-V_g$ curve of each . value respectively corresponding to the first ~~gate~~

voltage, the second ~~gate~~ voltage and the third ~~gate~~ voltage versus the first ~~gate~~ voltage, the second ~~gate~~ voltage and the third ~~gate~~ voltage, a reference $-V_g$ curve for the unstress-induced oxide layer is compared
5 with the $-V_g$ curve to monitor the quality of the oxide layer.

40. (Currently amended) The method of claim 39 wherein the $-V_g$ curve comprises at least a first region (region
10 I), a second region (region II), and a third region (region III).

41. (Currently amended) The method of claim 40 wherein the . value within the first region is zero to represent
15 each ~~gate~~ leakage current flowing through the first gateconductive layer being less than a predetermined current value, the absolute value of the . value within the second region increases to represent the stress-induced leakage current (SILC) resulting in the
20 increase of each ~~gate~~ leakage current flowing through the first gateconductive layer, the . value within the third region crosses the reference $-V_g$ curve to represent a plurality of carriers being trapped by the oxide layer.

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42. (Original) The method of claim 41 wherein the predetermined current value is $1.0 \times 10^{-11} \text{A}$.

43. (Currently amended) The method of claim 32 further
30 comprises ing a step for plotting a $-V_g$ curve of each . value versus each ~~gate~~ voltage, a reference $-V_g$ curve for the unstress-induced ~~tunnel~~ oxide layer in the

~~memory cell~~ is compared with the $-V_g$ curve to monitor
the quality of the ~~tunnel~~ oxide layer.